
TITLE

Hardware Synthesis of Complex System-on-Chip-Designs for Embedded Systems Using a Behavioural Programming and Multi-Process Model

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ABSTRACT

Embedded Systems used for control, for example in Cyber-Physical-Systems (CPS), perform the monitoring and control of complex physical processes using applications running on dedicated execution platforms in a resource-constrained manner. Traditionally program-controlled multi-processor architectures are used to provide the execution platform.

There are two different ways to model and implement System-on-Chip-Designs (SoC) used in those embedded systems: using 1. a structural and/or 2. a behavioural level. The structural level decomposes a SoC into independent submodules - processor cores, memories and peripherals - interacting with each other using centralized or distributed networks and communication protocols. The behavioural level usually describes the behaviour of the full design interacting with the environment, generally a more sophisticated modelling level. In the context of CPS these are mainly reactive systems with dominant and complex control paths. The major contribution to concurrency appears on control

path level.

A new SoC-design methodology is presented using the behavioural hardware compiler ConPro providing an imperative programming model based on concurrent communicating sequential processes (CSP) with an extensive set of interprocess-communication primitives. The programming language and the compiler-based synthesis process enables the design of constrained power- and resource-aware embedded systems with pure Register-Transfer-Logic efficiently mapped to FPGA and ASIC technologies. Concurrency is modelled explicitly on control- and data path. Additionally, concurrency on data path level can be explored and optimized automatically by different schedulers. The CSP programming model can be synthesized to different other levels, not only used for hardware circuit synthesis: software models (C, ML), intermediate mCode, RTL state level, and finally VHDL. The C and ML output enables a common source for both hardware and software implementation with identical functional behaviour.

An extended case study of a communication protocol used in high-density sensor-actuator-networks should demonstrate the design of a SoC for a robot actuator. The communication protocol is suited for high-density intra- and interchip networks.