TITLE

Smart Energy Management and Low-Power Design of Sensor and Actuator Nodes on Algorithmic Level for Self-Powered Sensorial Materials and Robotics

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ABSTRACT

Today there is an increasing demand for miniaturized smart sensors embedded in sensorial materials and smart actuators in microsystem applications. Each sensor and actuator node provides some kind of sensor, electronics, data processing, and communication. With increasing miniaturization and sensor-actuator density, decentralized network and data processing architectures are preferred. But energy supply is still centralized. Using local energy-harvesting technologies, a decentralized energy supply can be provided, too. Energy harvesting, for example using thermo-electrical sources, delivers actually only low electrical power, requiring 1. smart energy management on the consumer side controlling the energy consumption, and 2. low-power design.

We propose and demonstrate a design methodology for embedded systems satisfying low power requirements suitable for self-powered sensor and actuator nodes. This design methodology focuses on 1. smart energy management at runtime and 2. application-specific System-On-Chip (SoC) design at design time, contributing to low-power systems on both algorithmic and technology level.

Smart energy management is performed spatially at runtime by a behaviour-based or state-action-driven selection from a set of different (implemented) algorithms classified by their demand of computation power, and temporally by varying data processing rates. It can be shown that power/energy consumption of an application-specific SoC design depends strongly on computation complexity.

A simple example in sensor data processing is a calculation of mean values and data trends. Calculation could be performed by direct processing of a full data array, reducing array size or by using moving average algorithm reducing the accuracy. Data trends

could be estimated by nonlinear curve fitting, linear regression or interpolation of the last two sample values. These algorithms trade in different performance properties regarding noise rejection vs. calculation effort.
Depending on the actual state of the system, the actual and estimated future energy deposit, suitable algorithms can be selected and executed optimizing the Quality-of-Service (QoS) and the balance between accuracy and economy.
Signal and control processing is modelled on abstract level using signal flow diagrams (Matlab & Simulink modelling and simulation environment). These signal flow graphs are mapped to Petri Nets to enable direct high-level synthesis of digital SoC circuits using a multi-process architecture with the Communicating-Sequential-Process model on execution level (ConPro High-Level synthesis framework). Power analysis using simulation techniques on gate-level provides input for the algorithmic selection during runtime of the system, leading to a closed-loop design flow. Additionally, the signal-flow approach enables power management by varying the signal flow and data processing rates depending on actual energy consumption, estimated energy deposit, and required Quality-of-Service.