

Smart Energy Management and Low-Power Design of Sensor and Actuator Nodes on Algorithmic Level for Self-Powered Sensorial Materials and Robotics

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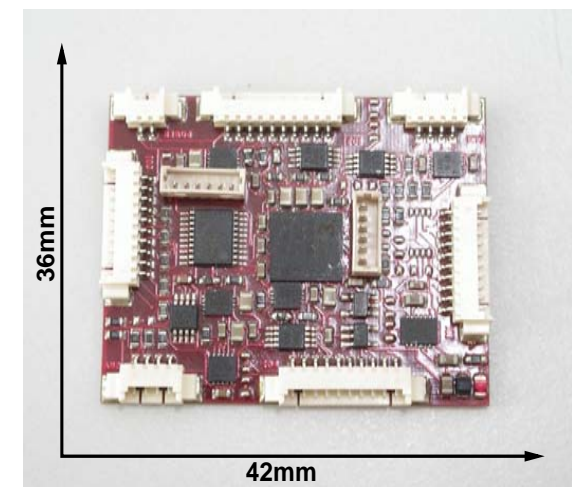
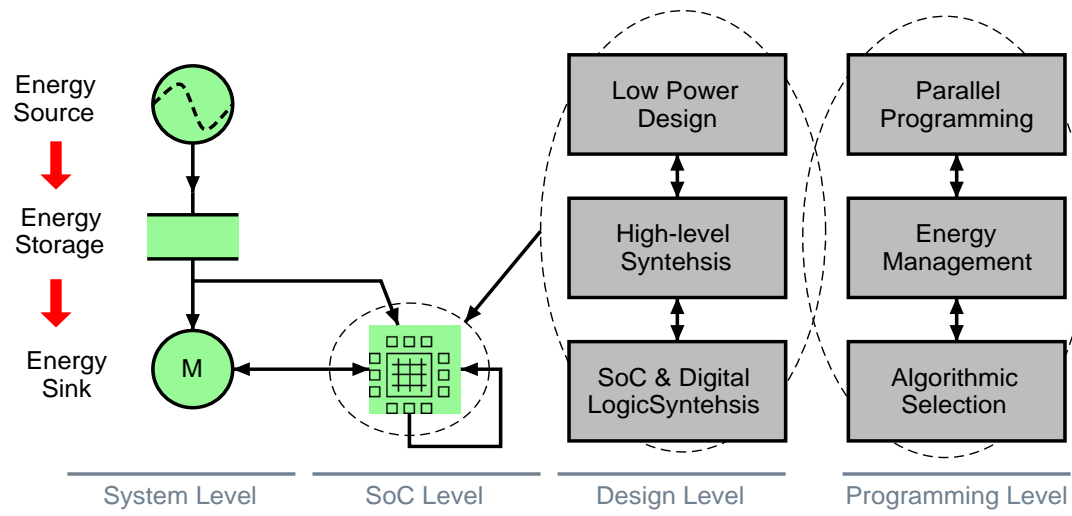
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Overview

Low-Power System Design and Energy Management on Algorithmic Level

1. Self-powered data processing systems for sensorial materials and robotics
2. **Low-power design**: Application-specific System-On-Chip design on algorithmic level using high-level synthesis
3. **Correlation of algorithmic complexity** and energy: Analysis of synthesized microchip activity, estimation of energy demand for computation
4. Technological extensions required for power reduction on microchip level
5. **Energy management** at runtime using **algorithmic selection** and dedicated methods from artificial intelligence and mapping to microchips
6. Preliminary simulation results



Self-powered data processing systems used in ...

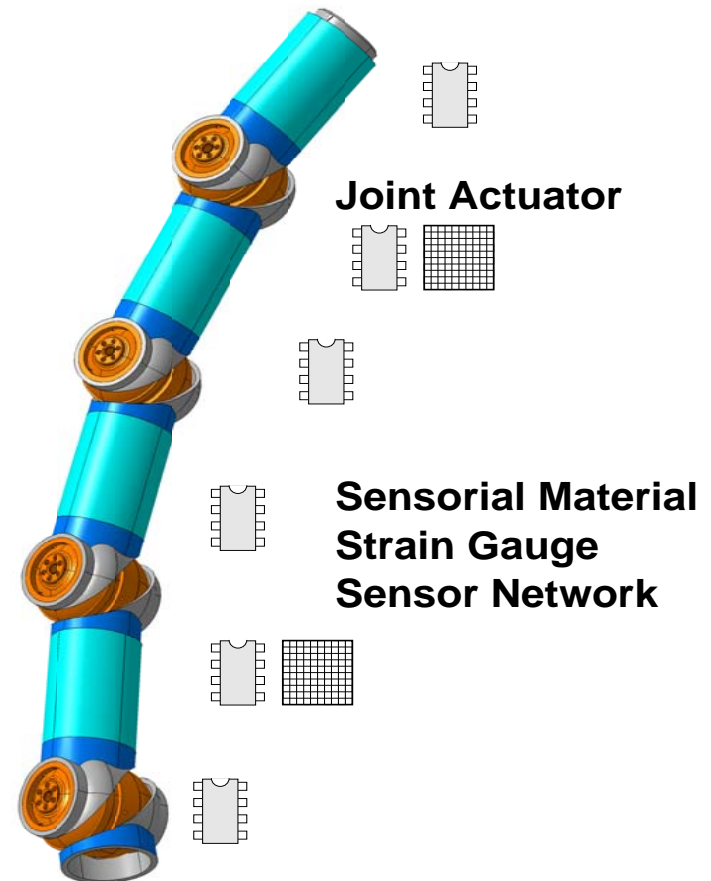
Cyber-Physical-Systems

- Defined by the interaction of the system with its environment
- Tight integration of computation and control with sensing and actuation physical components
- System components: sensors, actuators, data processing, communication → application specific
- CPS must be reliable, adaptable, easy-to-use, and low-power
- **Operation defined on algorithmic level - requires concurrency**

Sensorial Materials

- Network of smart sensor nodes
- Sensor node: sensor, electronics, and data processing
- SM must be reliable, adaptable, highly minaturized, and low-power

Figure 1. ModuACT robot arm manipulator with network of sensorial materials and actuator joints



ConPro: Programming Language & Highlevel-Synthesis

Synthesis of parallel application-specific System-On-Chip designs on programming level targeting FPGA and ASIC technologies

Programming Model & Language

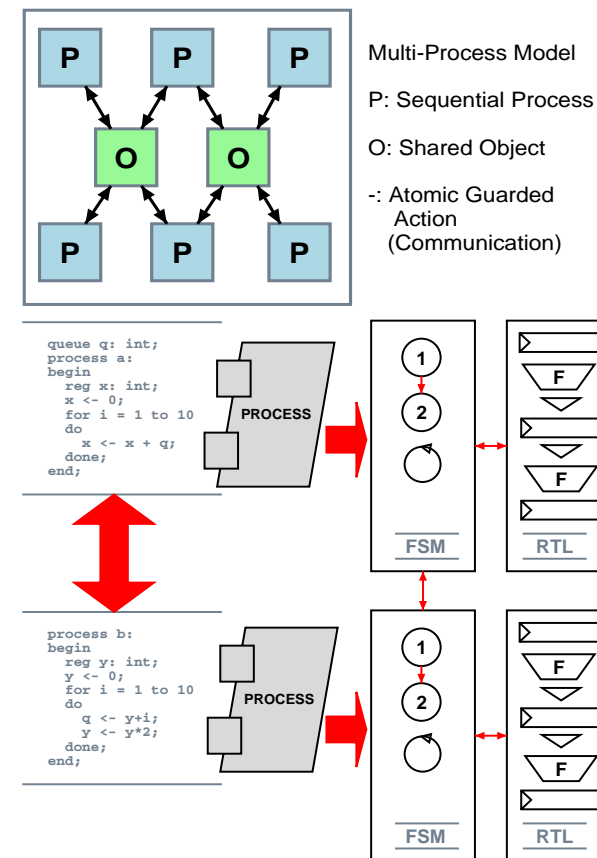
- Communicating Sequential Processes
- Imperative Language with explicitly modelled parallelism
- Guarded shared objects (atomic guarded access)
- Object orientated access of hardware blocks
- Concurrency on control- and data-path level
- Synchronization and Interprocess-Communication \Rightarrow directly implementable in hardware

Execution Model

- Process: strict sequential
- Mapped to Finite-State-Machine &

Register-Transfer Logic

Figure 2. Multi-Process Model [mod. CSP/Hoare]



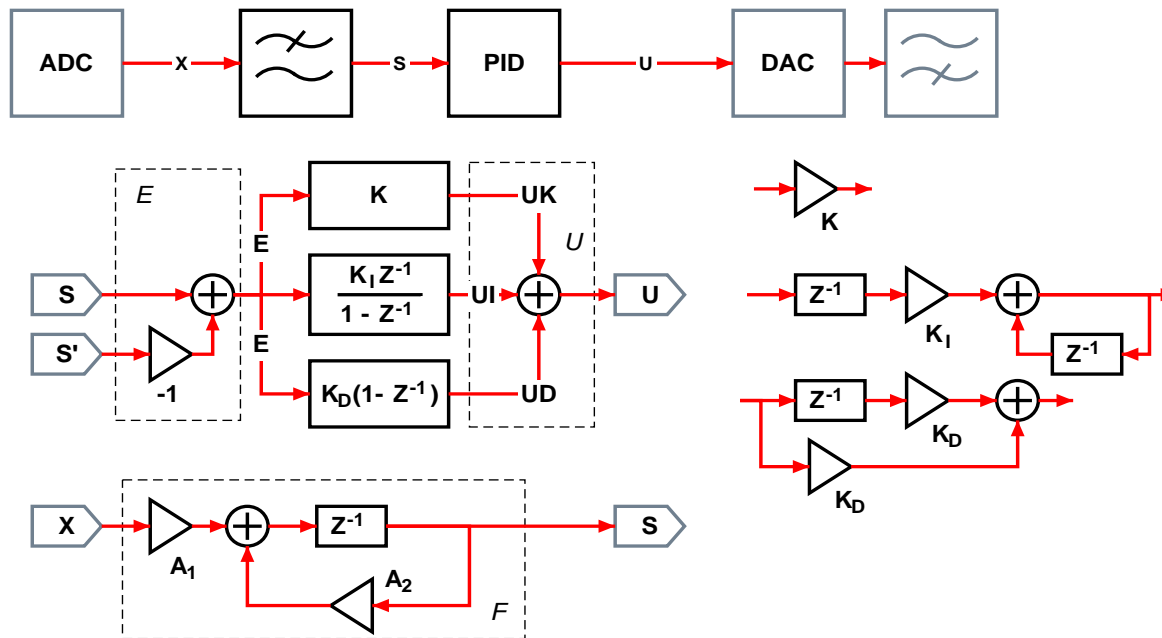
Modelling of Data Processing Systems

Modelling of parallel data processing systems using signal flow diagrams is an entry level for high-level synthesis on programming level

Signal Flow Diagrams

- Data processing is performed by using operational blocks on a sequential flow of discrete data sets
- Operational blocks: low level (simple arithmetic and relational operations), high-level (complex computation blocks), storage (delay)

Example 1. A PID controller modelled with signal flow diagrams



Mapping of Signal Flow Graphs to Petri-Nets

The signal flow graph is mapped to an intermediate representation to derive communication architecture, initial setup, and to explore concurrency

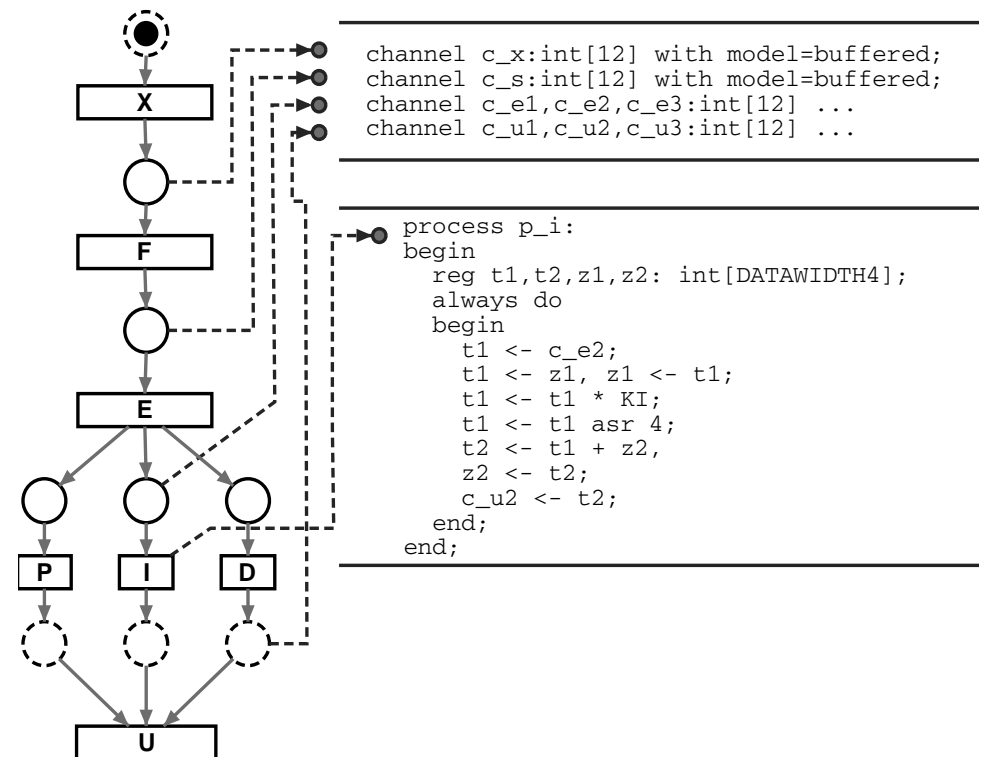
► Petri Nets

- Functional blocks are mapped to transitions
- States represent data which is exchanged between functional blocks
- The partitioning of functional blocks to transitions can be performed on different complexity levels
- Forked transitions provide mapping to concurrent data processing

► Programming Model

- Transitions are mapped to concurrently executing processes
- States are mapped to communication channels

Figure 3. Mapping of Petri-Net to multi-process programming model & ConPro language



Design Flow

A closed-loop design flow enables the design of optimized low-power embedded systems

- ▼ Specification of data processing system using signal flow graphs
- ▼ Mapping of signal flow graphs to Petri Nets
- ▼ Synthesis of Petri Net IR to processes and communication using ConPro programming model and language
- ▼ Synthesis of embedded SoC design on RT level
- ▼ Gate-level synthesis of SoC using standard cell library
- ▼ Event driven gate-level simulation provides input for power analysis (activity traces)
- ▼ Activity and power analysis of SoC provides input for Smart Energy Management

Figure 4. Closed-loop design flow using a graph-based virtual database environment

