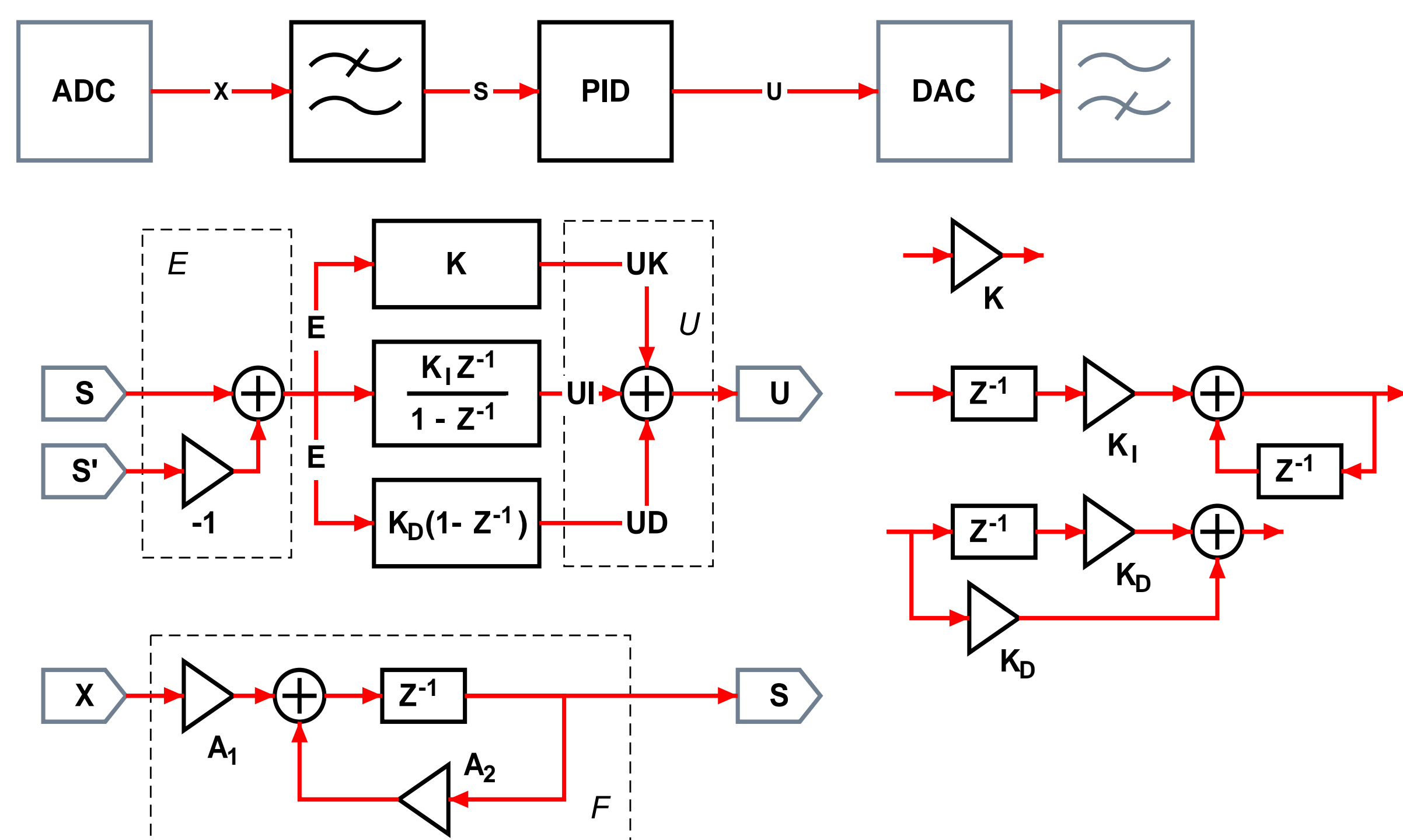


ENERGY-AWARE DESIGN FLOW FOR EMBEDDED SYSTEMS

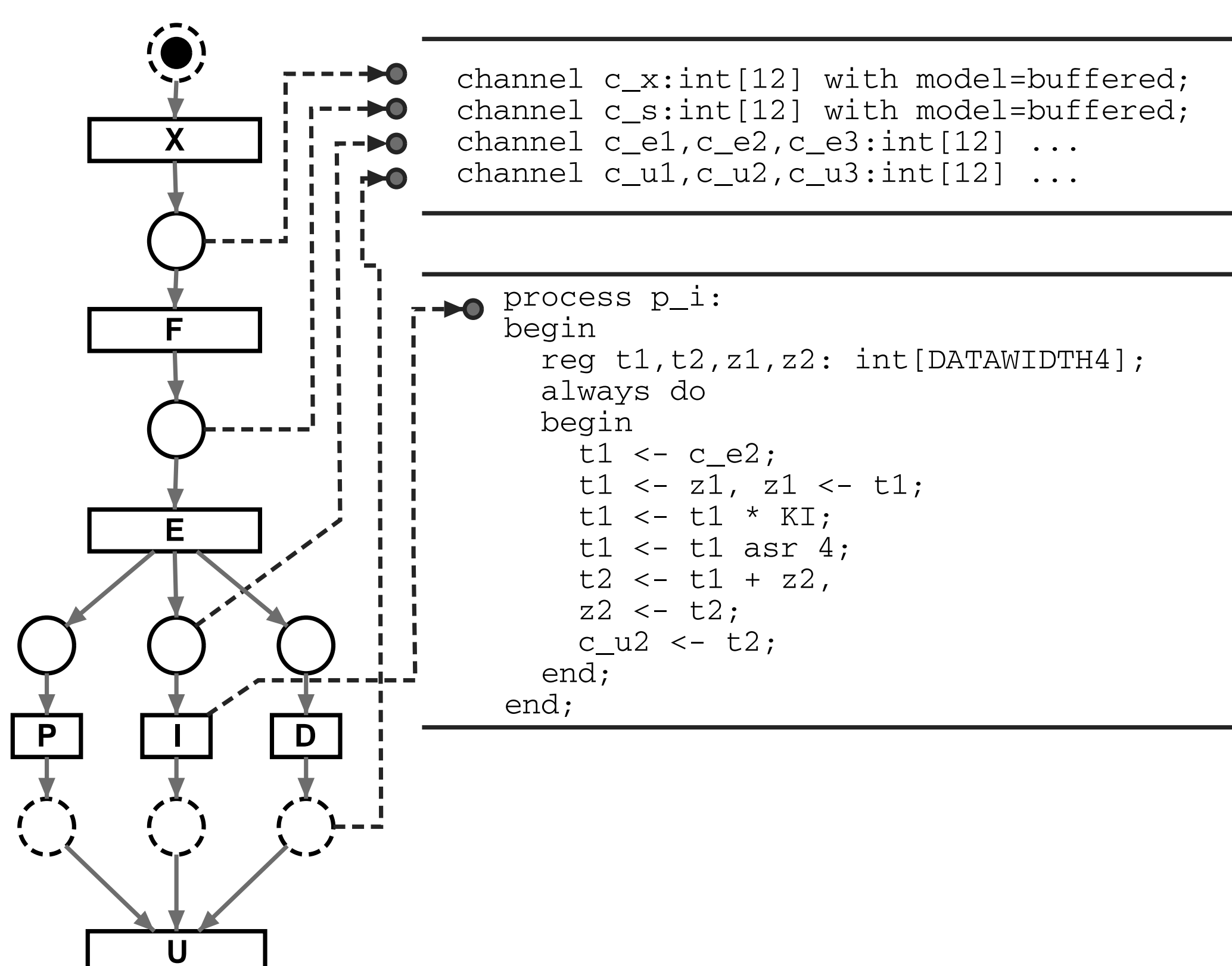
- Today there is an increasing demand for miniaturized smart sensors embedded in sensorial materials.
- With increasing miniaturization and sensor-actuator density, decentralized network and data-processing architectures are preferred, but energy supply is still centralized. *Advanced smart low-power design methodologies and applications are required.*
- A new design methodology focuses on 1. smart energy management at runtime and 2. application-specific System-On-Chip (SoC) design at design time contributing to low-power systems on both algorithmic and technological level.

Figure 1. Composition and modelling of a feedback-controlled system with signal flow diagrams. This example implements a PID controller used for example in actuator position control, consisting of sensor signal acquisition (ADC), filtering, and an error controller with a proportional, integral, and differential sub-controller [3].



- Data processing systems are modelled using signal flow diagrams (see **Figure 1.**) [2].
- This initial specification is used to derive 1. a multi-process programming model, and 2. a hardware model for a System-On-Chip design on Register-Transfer level.
- The signal flow diagram is first transformed into a S/T Petri Net representation (**Figure 2.**). The **Petri Net** is used 1. to derive the communication architecture, and 2. to determine an initial configuration for the communication network.
- The Petri Net is mapped to sequential processes performing functional operations and channels providing the inter-process communication.
- Finally, a RTL SoC design is synthesized [1] and the circuit activity is analyzed regarding different algorithms and complexity (**Figure 4.**).

Figure 2. Mapping of the signal flow diagram to a Petri Net and mapping of Petri Net to communication channels and sequential processes using the ConPro programming language.



ENERGY MANAGEMENT AT RUNTIME

- Smart energy management is performed spatially at runtime by a behaviour-based or state-action-driven selection from a set of different (implemented) algorithms classified by their demand of computation power, and temporally by varying data-processing rates (*based on previous activity analysis*).

Definition 1. Constraints net relations satisfying quality of service and minimizing power consumption to be fulfilled at runtime. Some values are derived from circuit activity analysis.

$VARs = \{Runtime, Rate, Level, Energy, Power, Error\}$
 $Runtime = \{LOW=1, MED=2, HIGH=3\}, Error = \{0, 5, 10, 100\}, Level = \{LOW=1, HIGH=1.5\},$
 $Rate = \{1, 5, 10, 50, 100\}, \dots$
 $Runtime > 0, Energy > 0, Rate > 0$
 $Energy \geq (Power * Runtime) / 2$
 $Power \geq (Level * Rate) / 4$
 $Error \leq (Level + Rate) / 2$

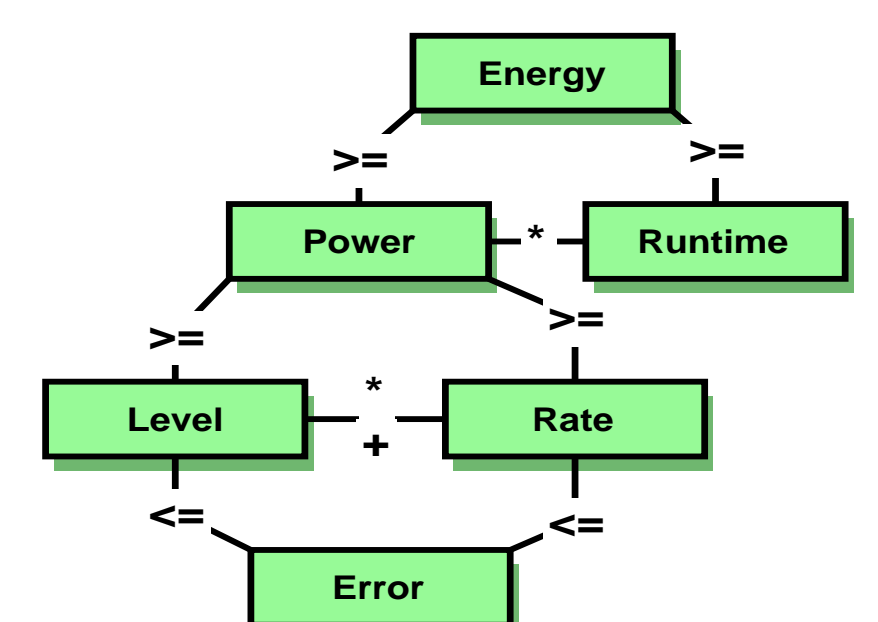
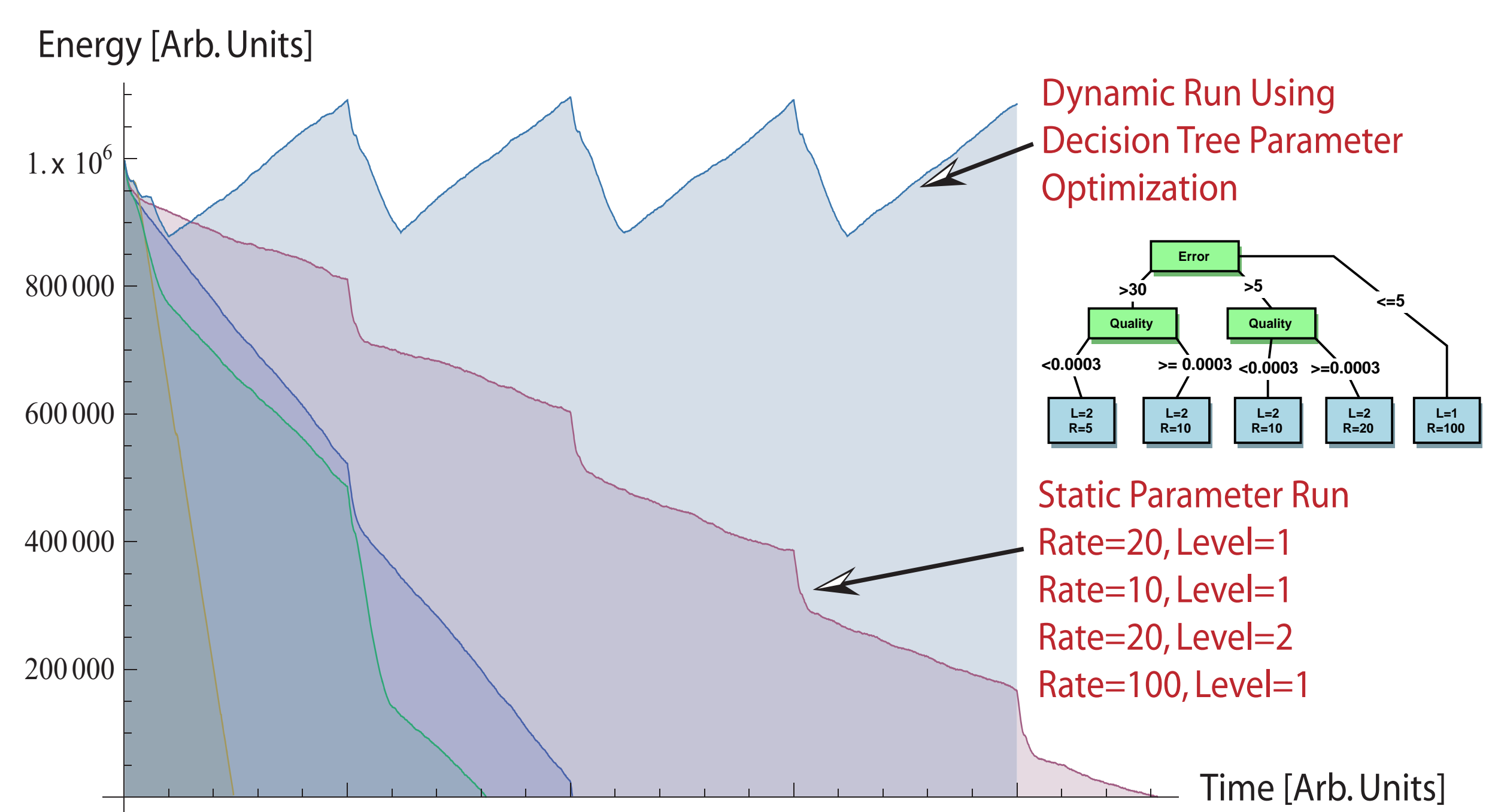
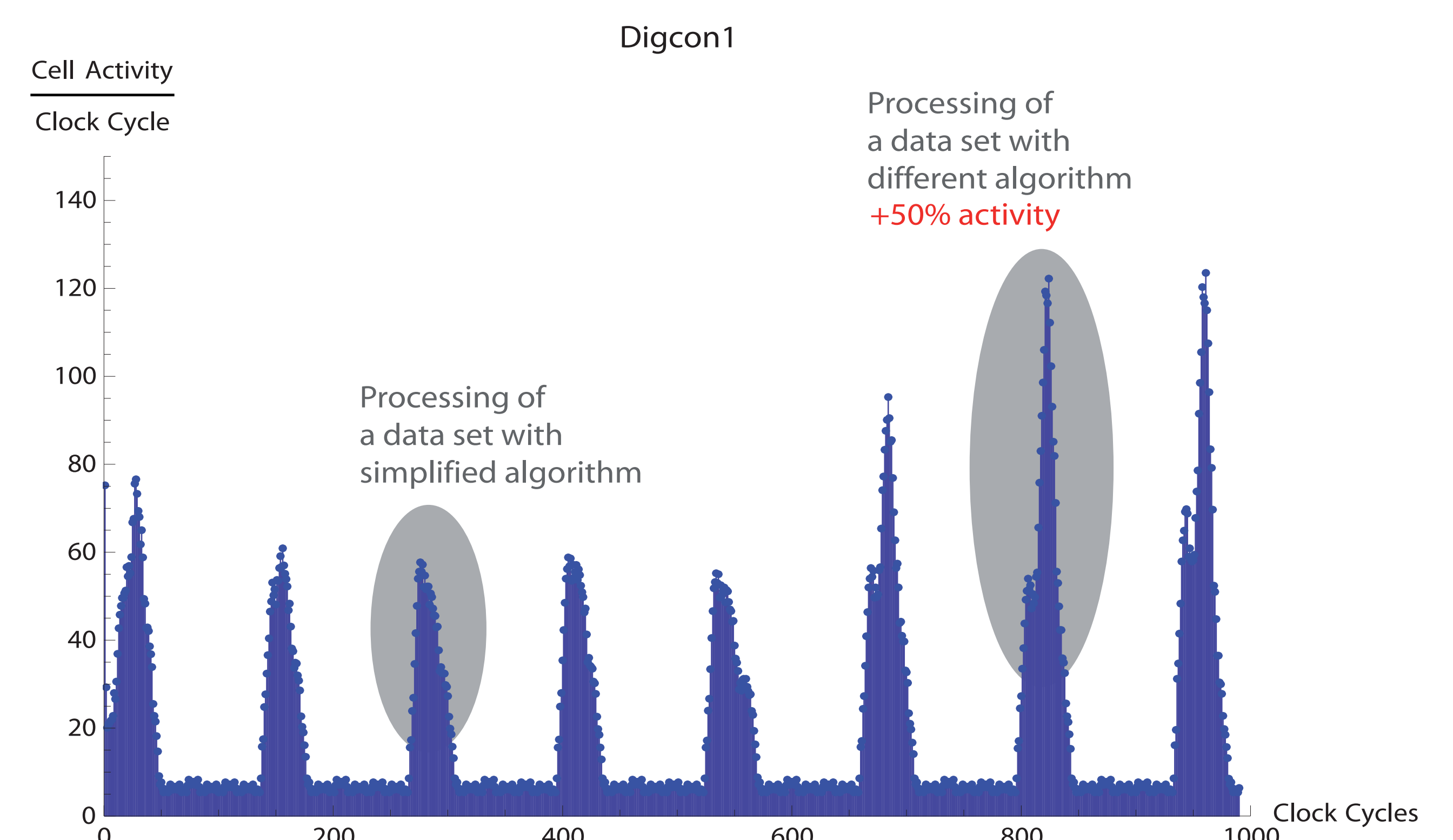


Figure 3. System simulation (from Figure 1.) with different runtime behaviours using a decision tree which can be retrieved by machine learning methods. Parameters: Data-processing rate={1,5,10,20,100}, Algorithmic level={P:1,PID:2}



- Using advanced methods from the **artificial intelligence** area enables dynamic adaption of smart sensors and actuators at runtime.
- Definition 1 shows a **constraints net** approach performing energy management at runtime.
- Figure 3.** shows simulation results of a system using **decision tree** and machine learning approaches to optimize the runtime behaviour.

Figure 4. SoC cell activity correlates strongly with computation and signal/data flow. The first five results are computed only with the P controller; after obtaining the fifth result value U, the I and D computational blocks are switched on.



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